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SYSTEMATIC EVALUATION OF THE EFFECT OF NANOWIRE DIAMETER ON SHORT CHANNEL EFFECTS IN SILICON NANOWIRE FIELD EFFECT TRANSISTOR

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ABSTRACT
The relentless scaling of transistor technology into the nanometer regime has exacerbated short-channel effects (SCEs), which significantly degrade device performance. Silicon nanowire field-effect transistors (Si-NWFETs) have emerged as promising candidates to mitigate these challenges due to their superior electrostatic control. However, the specific influence of a key geometric parameter, the nanowire diameter on SCEs remains inadequately explored and demands a thorough investigation. This study employs numerical simulations using the MuGFET tool's PADRE simulator to systematically evaluate the effect of silicon nanowire diameter, varied from 2 nm to 12 nm, on key SCE metrics and performance parameters. The results demonstrate a strong positive correlation between diameter and detrimental SCEs: drain-induced barrier lowering (DIBL) increases from 0.50 mV/V to 15.22 mV/V, and the subthreshold swing (SS) degrades from 75.23 mV/dec to 91.08 mV/dec as the diameter expands. Conversely, the threshold voltage exhibits a roll-off, decreasing from 0.73 V to 0.48 V with increasing diameter. Furthermore, the drain current and transconductance show a significant linear enhancement, improving by over five times, which is advantageous for drive strength and analog performance. This work reveals a critical performance trade-off: smaller diameters (2 nm) are optimal for electrostatic integrity and minimizing SCEs, while larger diameters (12 nm) are essential for achieving high on-current, transconductance, and switching speed. These findings provide vital design insights for optimizing Si-NWFET performance for specific applications and guiding future technology scaling.

Keywords: **Drain-Induced Barrier Lowering (DIBL), Electrostatic Control, Nanowire Diameter, Silicon Nanowire FET (Si-NWFET), Transconductance**

1.0 INTRODUCTION
The continuous downscaling of transistor technology into the nanometer regime has introduced critical challenges collectively referred to as short-channel effects (SCEs) [1], [2], [3]. Prominent examples of these effects include drain-induced barrier lowering (DIBL), subthreshold swing (SS), and threshold voltage variation, all of which degrade MOSFET performance and compromise device reliability. To address these limitations, nanowire field-effect transistors (NWFETs) have emerged as promising candidates for extending MOSFET scaling. Their ability to provide superior electrostatic control and enhanced current drive has attracted significant research attention worldwide. The rapid growth of nanowire research is driven by multiple factors. One major reason is that semiconductor nanowires can be produced in large quantities with consistent electronic properties, making them suitable for large-scale integrated systems [4]. Moreover, the quasi-one-dimensional conduction in nanowires enhances carrier transport efficiency, reinforcing their suitability for next-generation nanoscale devices. Consequently, numerous studies have focused on silicon nanowire FETs (Si-NWFETs) [5], [6], [7], [8], [9], [10]. Despite this progress, the influence of critical geometric parameters particularly nanowire diameter on short-channel effects has

not been investigated in sufficient detail. A systematic evaluation of how nanowire diameter alone impacts SCEs is essential, as it provides valuable design insights for optimizing Si-NWFET performance and guiding technology scaling. This gap motivates the present simulation-based study, which aims to quantify and analyze the relationship between nanowire diameter and SCEs; DIBL, SS, threshold voltage variation alongside other important metrics such as on-current and transconductance using PADRE simulator from MuGFET tool, thereby supporting the development of more reliable and energy-efficient nanoscale transistors.

2.0 THEORETICAL BACKGROUND

This section discusses the si-NWFET structure and short channel effects.

2.1 Device Structure

Figure 1 shows the Si-NWFET's device architecture. The source, drain, gate, and gate oxide are some of its crucial components. The source and drain represent the charge injection and collecting regions, respectively, and the gate is the control terminal that alters the carrier flow across the nanowire channel. When positioned between the gate electrode and the channel, the gate oxide provides the necessary insulation and enables effective electrostatic control over the channel. Together, these components define the Si-NWFET's operating characteristics and are crucial for defining its performance and short-channel behavior.

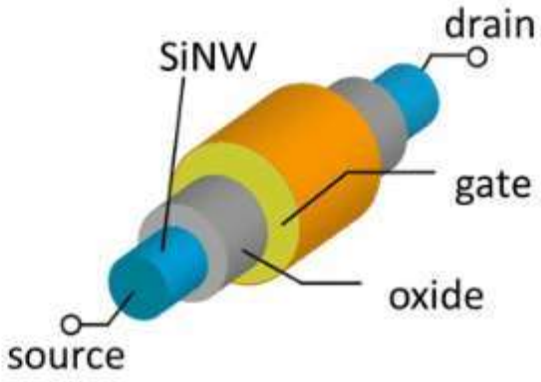

Figure 6: Si-NWFET Device Structure [11].

2.3 Short Channel Effects (SCEs)

Short channel effects deteriorate the device performance. There are several types of short channel effects, some of which are:

(a) Drain-Induced Barrier Lowering (DIBL):
The increase in drain voltage from 0.01 V to 0.05 V causes a variation in threshold voltage. This is referred to as drain induced barrier lowering. It is one of the most critical short channel effects. The DIBL value can be determined using [12]:

$$DIBL(\frac{mV}{V}) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (1)$$

where V_{TH} denotes threshold voltage and V_{DS} denotes drain-source voltage.

(b) Subthreshold Swing (SS): The subthreshold swing parameter, one of the SCEs, for a Multigate Field Effect Transistor is usually 60 mV/dec. The SS can be calculated by [13]:

$$SS\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (log_{10}\ I_{DS})} \quad (2)$$

where V_{GS} denotes gate-source voltage and I_{DS} denotes drain-source current.

(c) Threshold Voltage: Assessing the threshold voltage of a device is a crucial step in determining its feasibility as a channel material for switching applications. The lowest gate voltage required to provide a conduction path between the source and the drain is known as the threshold voltage [14]. The threshold voltage of a FinFET device can be calculated using [15]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (3)$$

where Q_{SS} denotes charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, f_{ms} denotes metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential, and V_{in} is the additional surface potential to $2f_f$ that is needed for ultrathin body devices to bring enough inversion charges in to the channel region of the transistor to reach threshold point [15].

3.0 METHOD

The simulations were carried out using the PADRE simulator, a module of the Multigate Field-Effect Transistors (MuGFET) tool, applied to a silicon Nanowire FET (Si-NWFET) device. This simulator is well-suited for generating detailed current–voltage characteristics that aid in understanding the fundamental physics of FET operation. It consistently solves the coupled Poisson and drift–diffusion equations [16], ensuring reliable device modeling. In this study, the effect of nanowire diameter variation, ranging from 2 nm to 12 nm, was investigated while keeping the gate length fixed at 20 nm and the oxide thickness at 2 nm. The channel doping concentration was maintained at 1×10^{16} cm^{-3}, with source and drain doping concentrations of 1×10^{19} cm^{-3}. The applied bias conditions included a drain voltage sweep from 0.05 V to 1 V and a gate voltage sweep from 0 V to 1 V.

4.0 RESULTS AND DISCUSSION

This section presents and discusses simulation results on the impact of silicon nanowire diameter variations on the short-channel effects (SCEs) in nanowire field-effect transistors (NWFETs). The study was conducted using the PADRE simulator within the MuGFET framework to evaluate key SCE metrics namely, drain-induced barrier lowering (DIBL), subthreshold swing (SS), and threshold voltage roll-off along with other performance parameters such as on-current and transconductance. The findings offer critical design insights for optimizing Si-NWFET performance and guiding future technology scaling.

4.1 Effect of Silicon Nanowire Diameter on Drain Induced Barrier Lowering

Figure 1 plots drain-induced barrier lowering (DIBL) against silicon nanowire diameter for the Si-NWFET. The results indicate a strong positive correlation between DIBL and diameter; DIBL increases from a minimum of 0.50 mV/V at a 2 nm diameter to a maximum of 15.22 mV/V at 12 nm. This trend is critical, as elevated DIBL directly promotes leakage current, thereby degrading device efficiency and electrostatic integrity. Consequently, the 2 nm nanowire diameter, which yields the minimal DIBL, is identified as the optimal design point for mitigating short-channel effects and enhancing overall device performance.

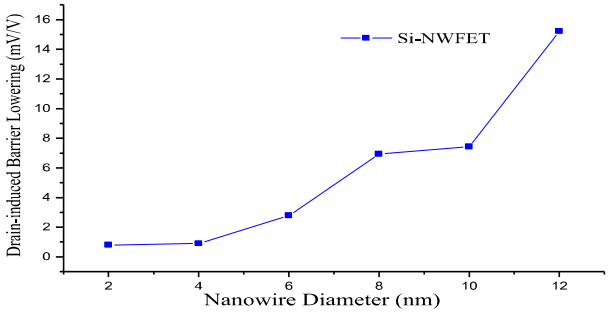

Figure 7: Graph of Drain-Induced Barrier Lowering against Nanowire Diameter

4.2 Effect of Silicon Nanowire Diameter on Subthreshold Swing

The optimal subthreshold swing (SS) of 75.23 mV/dec was achieved at a 2 nm nanowire diameter, as evidenced by the data in Figure 2. Beyond this point, a pronounced degradation in switching efficiency is observed, with SS worsening to 91.08 mV/dec at 12 nm. This substantial increase underscores a deterioration in electrostatic control, which directly elevates leakage current and compromises device performance. Therefore, minimizing the nanowire diameter is significant for preserving a sharp subthreshold slope and mitigating short-channel effects.

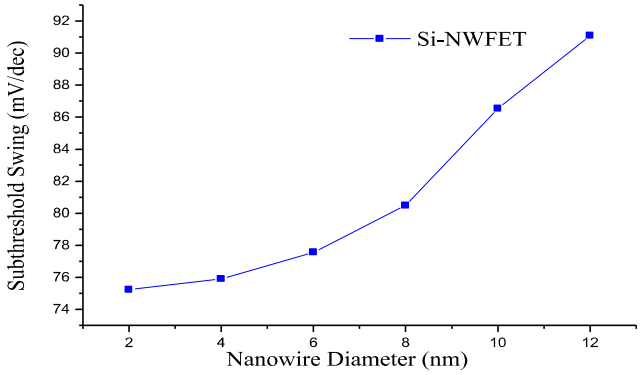

Figure 8: Graph of Subthreshold Swing against Nanometer Diameter

4.3 Effect of Silicon Nanowire Diameter on Threshold Voltage

Figure 3 illustrates the inverse relationship between silicon nanowire diameter and threshold voltage in the Si-NWFET. As the diameter scales down from 12 nm to 2 nm, threshold increases from 0.48 V to 0.73 V. This roll-off in threshold voltage with increasing diameter is a critical short-channel effect that, while beneficial for lowering operating voltage and improving switching speed, must be carefully managed to avoid excessive leakage and a loss of gate control. The results suggest a performance trade-off, where larger diameters (12 nm) favor dynamic power and speed, while smaller diameters enhance electrostatic integrity.

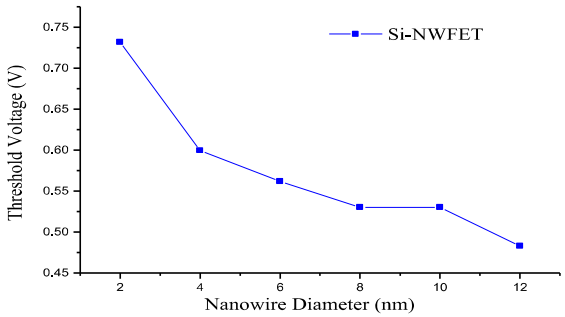

Figure 9: Graph of Threshold Voltage of against Nanowire Diameter

4.4 Effect of Silicon Nanowire Diameter on Drain Current

Figure 5 demonstrates a linear increase in drain current with nanowire diameter in the si-NWFET, rising from 1.45×10^{-5} A/μm at 2 nm to 7.75×10^{-5} A/μm at 12 nm. Key performance metrics will benefit greatly from this increase in current carrying capacity. First and foremost, a superior on-state current, a key performance metric for transistors is directly correlated with a higher drain current. In digital circuits, a high on-state current is essential because it allows load capacitances to be charged and discharged more quickly, which greatly increases transistor switching speed and decreases circuit delay. Furthermore, this increased drain current is intrinsically linked to higher transconductance, which reflects the device's amplification efficiency and gain. These findings unequivocally show that improving device performance requires designing with larger nanowire diameters. This demonstrates how a larger diameter clearly improves the performance of digital circuits, but at the expense of worsened electrostatic control.

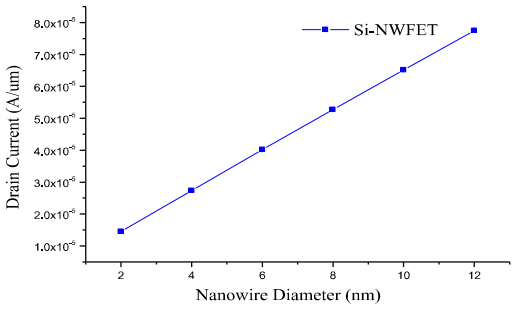

Figure 10: Graph of Drain Current against Nanowire Diameter

4.5 Effect of Silicon Nanowire Diameter on Transconductance

Figure 6 illustrates the definitive relationship between transconductance and nanowire diameter, revealing a strong linear augmentation as the diameter is scaled from 2 nm to 12 nm. This trend is a direct correlate of the drain current behavior shown in Figure 5, fundamentally because transconductance is the derivative of drain current, making its value inherently dependent on the drain current level. The data shows a pronounced improvement, with transconductance reaching a maximum value of 4.64×10^{-4} S/μm at the largest diameter of 12 nm. This enhancement in transconductance is a critical performance indicator. A higher transconductance value signifies a greater change in output current for a

given change in input gate voltage, which is the fundamental mechanism of amplification. Therefore, the observed increase directly translates to superior amplification gain, improved linearity, and more efficient signal processing capabilities in the transistor.

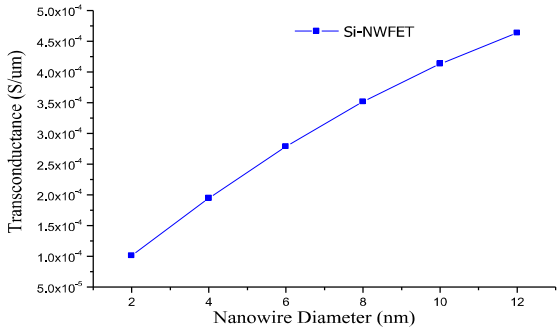

Figure 11: Graph of Transconductance against Nanowire Diameter

Consequently, these findings have significant implications for circuit design. For high-frequency and analog applications such as low-noise amplifiers (LNAs), operational amplifiers (op-amps), and radio frequency (RF) circuits. Optimizing the nanowire diameter to maximize transconductance is paramount. A larger diameter is shown to be essential for achieving the desired high gain, robust drive strength, and optimized frequency response, thereby enabling higher-performance analog and mixed-signal systems.

5.0 CONCLUSION

This simulation-based study systematically evaluated the impact of silicon nanowire diameter on the performance and short-channel effects (SCEs) of Si-NWFETs, revealing a critical design trade-off between electrostatic integrity and drive capability. The key finding is that the nanowire diameter is a pivotal geometric parameter that directly dictates this trade-off. Smaller diameters, specifically provide superior electrostatic control, yielding minimal drain-induced barrier lowering and a near-ideal subthreshold swing, making them optimal for low-leakage, high-efficiency switching applications. Nevertheless, this results in lower transconductance and drive current. On the other hand, larger diameters greatly improve performance metrics, increasing transconductance and drain current five times, which is beneficial for high-speed digital and high-gain analog circuits. However, this improvement is accompanied by a significant deterioration in electrostatic control, as shown by a noticeable threshold voltage roll-off, a high DIBL, and a degraded SS. As a result, the ideal nanowire diameter depends entirely on the application and cannot be determined universally. This study offers important design insights and concludes that while maximizing the diameter is required to achieve high performance and drive strength, minimizing the diameter is necessary to mitigate SCEs and maximize energy efficiency. These findings provide clear guidelines for optimizing future nanoscale transistor technologies. Additionally, to evaluate manufacturability and application range, critical studies on reliability such as variability, self-heating, and bias temperature instability as well as the performance at cryogenic temperatures for quantum computing are crucial.

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PERFORMANCE COMPARISON OF MODEL PREDICTIVE CONTROL (MPC) AND NONLINEAR PID (NPID) FOR BLDC MOTOR SPEED CONTROL

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ABSTRACT
The utilization of Brushless Direct Current (BLDC) motor in real world is undoubtedly growing because of their high efficiency, low maintenance requirements, minimal noise level, and reliability. Nevertheless, nonlinearities and parameter uncertainties make the system control a bit harder. Similarly, a study comparing the effectiveness of the two promising controllers is limited. Model Predictive Control (MPC) which have been known due to their ability in predicting the future behavior of a system (motor) and accommodating of constraints Also, Nonlinear PID (NPID) which was an upgraded version of conventional PID so as to handles the system nonlinearities and uncertainties. This study presents a comparative evaluation of Model Predictive Control (MPC) and Nonlinear PID (NPID) for regulating the speed of a BLDC motor. A comprehensive transfer function which captures both electrical and mechanical dynamics of the system was formulated from the mathematical model and the controllers were both developed and analyzed in MATLAB/Simulink. The performance metrics which includes rise time, settling time, and overshoot percentage are measured. The simulation outcomes highlights that the NPID demonstrates a quicker response, while the MPC reduces overshoot and a smoother transient performance. Additional input signals, such as sine waveform, square waveform, and ramp were applied to evaluate the tracking capability, revealing that NPID possess a slightly better tracking ability under all the conditions. This finding reveals the ability of both advanced control algorithms in addressing the nonlinearities and parameter uncertainties of the motor.

Keywords: Brushless DC motor (BLDC), Model Predictive Control (MPC), MATLAB/Simulink, Nonlinear PID (NPID), Speed Regulation.

1.0 INTRODUCTION
The proper regulation of an electric motor heavily depends on effective controllers to ensure accuracy, stability, and efficient operation, most especially when motors under varying loads, or environmental factors. However, the implementation of such effective controllers is difficult due to the electric motors nonlinearity and parameter uncertain, which simply means their meaning their output does not remain constant across all operating conditions. Furthermore, the motor's internal parameters such as resistance R, inductance I, and back-EMF constants usually varies due to factors like temperature, aging, or humidity, causing the system control more challenging. Brushless DC (BLDC) motors faces more of the difficulties listed above because of its nonlinear characteristics. Therefore, the motor needs an effective control technique that can handles the changes properly without causing instability or an overshoot. Due to this, BLDC motor speed control really requires an authentic and highly robust controllers capable of handling those factors. [1][2].

Several attempts were made by research contributors to counter the problem which includes Classical controllers such as Proportional-Integral-Derivative (PID) and Proportional-Integral (PI), are widely tested for BLDC motor speed regulation because of their implementation simplicity [3][4]. However, the controllers deteriorated when dealing with nonlinear system like BLDC motor. Intelligent controllers such as ANFIS [5], ANN [6] and Fuzzy logic [7] were all applied for BLDC motor speed control due their robustness and accuracy. However, rules formations, computational intensive, interpretation and tuning difficulties are their major problems.

Advanced controllers such as Model Predictive Control (MPC) and Nonlinear PID (NPID) are capable of handling multi input and multi output system (MIMOS) and nonlinear system such as BLDC motor to achieve a proper speed regulation [8][9]. A report on effectiveness and the capabilities of the two advanced controllers under same condition is limited.
This research presents a performance comparison of MPC and NPID controllers for BLDC motor speed control using MATLAB/Simulink. Furthermore, this study contributes to the body of knowledge by offering recommendations for selecting appropriate controllers based on system requirements.

1.1 **Theoretical Background**

The section discusses on the theories and the equation governing the study

1.1.1 Mathematical Modelling of BLDC Motor

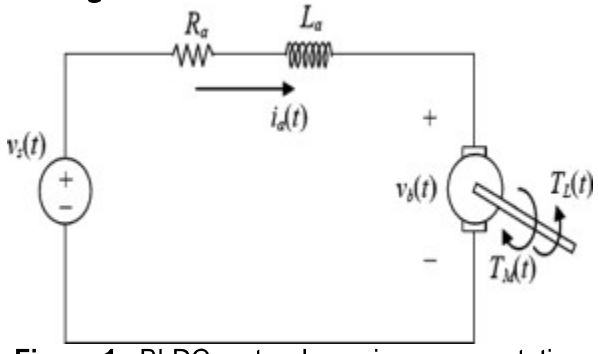

Figure 1. BLDC motor dynamics representation

The BLDC motor diagram described R_a= armature resistance, L_a = armature inductance, I_a = armature current, m = motor, j = rotor inertia, f = viscous friction, w = angular Velocity, θ = angular position.
From Faraday's law of electromagnetic induction, the back electromotive force (EMF) is proportional to the angular velocity ωm (rad/s).

$$E_B = K_B w_m(t) \quad (1)$$

The motor Torque T_m is proportional to the armature current i_a by a Torque constant K_t from the Lorentz force.

$$T_m(t) = K_t\, i_a(t) \quad (2)$$

The mechanical operation of the BLDC motor

$$T_{m} = J\frac{dw_m}{dt} + f_m w_m + T_L \quad \text{But the Torque load (} T_L \text{) is considered zero} \quad (3)$$

The voltage across the armature resistance, inductance, and back EMF is given as

$$E_a(t) = R_a i_a(t) + L_a \frac{di_a}{dt} + E_b(t) \quad (4)$$

In S-domain equation 5 becomes.

$$E_a(\text{s}) = R_a i_a(s) + SL_a i_a(s) + E_b(s) \quad (5)$$

The armature current derived from equation (5) to s-domain is given as

$$i_a(s) = \left(\frac{1}{L_{as}+R_a}\right)(E_a(s) - E_b)(s) \quad (6)$$

The motor Torque T_m shown in equation (2) in time domain is now converted to S-domain given as

$$T_m(\text{s}) = K_t\, i_a(\text{s}) \quad (7)$$

The mechanical dynamics of the motor given in equation (3) is now converted to S-domain which is given as

$$T_{m = Jsw(s)} + \text{f w(s)} + T_L \quad \text{Since, } T_L = 0 \quad (8)$$

To obtain the angular velocity (w) in S-domain is given as

$$T_{m} = (Js + f)\, w(s) \quad (9)$$

Angular velocity (w) in S-domain is given as

$$w(s) = \frac{1}{(js+f)} T(s) \quad (10)$$

The back EMF E_b from equation (1) in Time domain is now derived in S-domain and is given as

$$E_b(s) = k_b w(s) \quad (11)$$

For the angular displacement (Θ) in S-domain is,

$\frac{d\theta}{dt} = w$ This implies sθ(s) = w(s)

$$\Theta(\text{s}) = \frac{1}{s}\, w(s) \quad (12)$$

The ratio of output to the input which is the transfer function of the BLDC motor is given by

$$\frac{\Theta(s)}{E_a} = \frac{k_t}{s\{(R_a + L_a s)(sJ+f) + k_t k_b\}} \quad (13)$$

The equation (13) shows the Transfer function of BLDC motor which comprises both the electrical and mechanical elements such as resistance R_a, torque constant k_t, inductance L_a, Back EMF k_b, viscous friction f, rotor inertia J, source voltage E_a according to [10].

1.1.2 Nonlinear PID (NPID)

The NPID controller was design to improve the control performance beyond that of conventional PID controller. The NPID controller modifies the proportional, integral, and derivative gains in such a way that the gain varies with time to handles the nonlinear behavior of the motor under varying conditions.

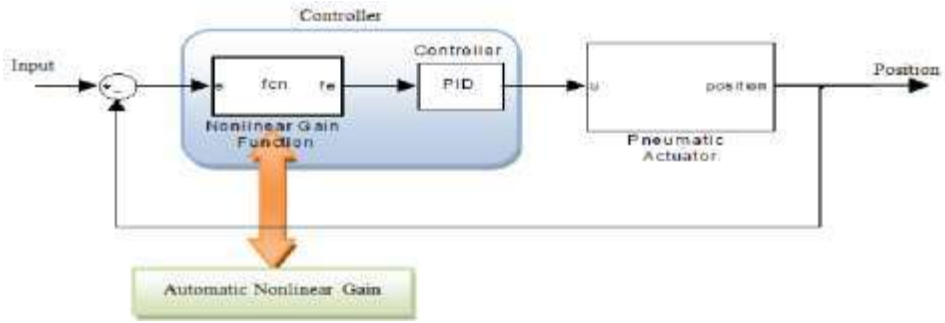

Figure. 2 Nonlinear PID block diagram [12].

The Matlab function block in the NPID block diagram shown in fig.2 contains the nonlinear gain function of the controller. These gain involves parameter such as the emax which is the maximum limit of the error, Ko which is the overall controller strength, the hyperbolic tangent function (tanh) and Alpha are meant to handles the aggressiveness of the system.

1.1.3 Model Predictive Control (MPC)

Model predictive control is a type of control algorithm that has been applied practically and through simulation means to handle different systems either complex or simple, linear or nonlinear and multi-input or multi-output (MIMO). The technique uses the process model to predict the future output response of a system. However, at each step, the control strategy tries to optimize plant behavior by adjusting the manipulated variable [13]. The controller's prediction capability combines with the classical feedback operation allows the algorithm to make adjustments for desired performance.

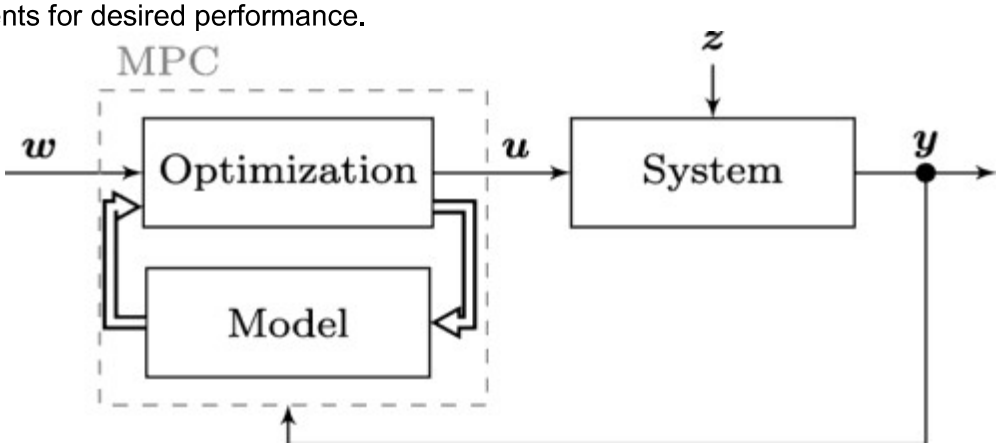

Figure 3. Simplified block diagram of a MPC-based control loop [8].

In designing an MPC controller, parameters such as control horizon (N), prediction horizon (P), model horizon (NM), sampling time (Ts), Weight factor and Constraints are very essential as this would lead to an effective and robust controller [14].

2. METHODOLOGY

The section discusses on the software environment, BLDC motor modeling, controller design, and simulation procedure.

2.1 Software Environment

This study considered the use MATLAB/Simulink as the key software environment for the design, and performance simulation of the controller. MATLAB/Simulink provides a high-capacity, model-based design framework that supports the development and analysis of complex dynamic systems with a high degree of numerical accuracy. Its computational robustness enables efficient handling of nonlinear models, iterative optimization routines,

and real-time response simulations required for advanced control strategies such as Model Predictive Control (MPC).

Among the features of the MATLAB/Simulink, it has library which contain some predefined blocks particularly those relating to electric drives, control algorithms, and system dynamics, allows for precise representation of the nonlinear behavior of BLDC motors. The software also enables parameter tuning tools, and a stable simulation environment, which reliable performance comparison between the MPC and NPID controllers. There MATLAB/Simulink software was considered due to its reliability and cost-free advantages, its suitability for both classical and advanced controller, and its ability to provide accurate result.

2.2 Simulation procedure

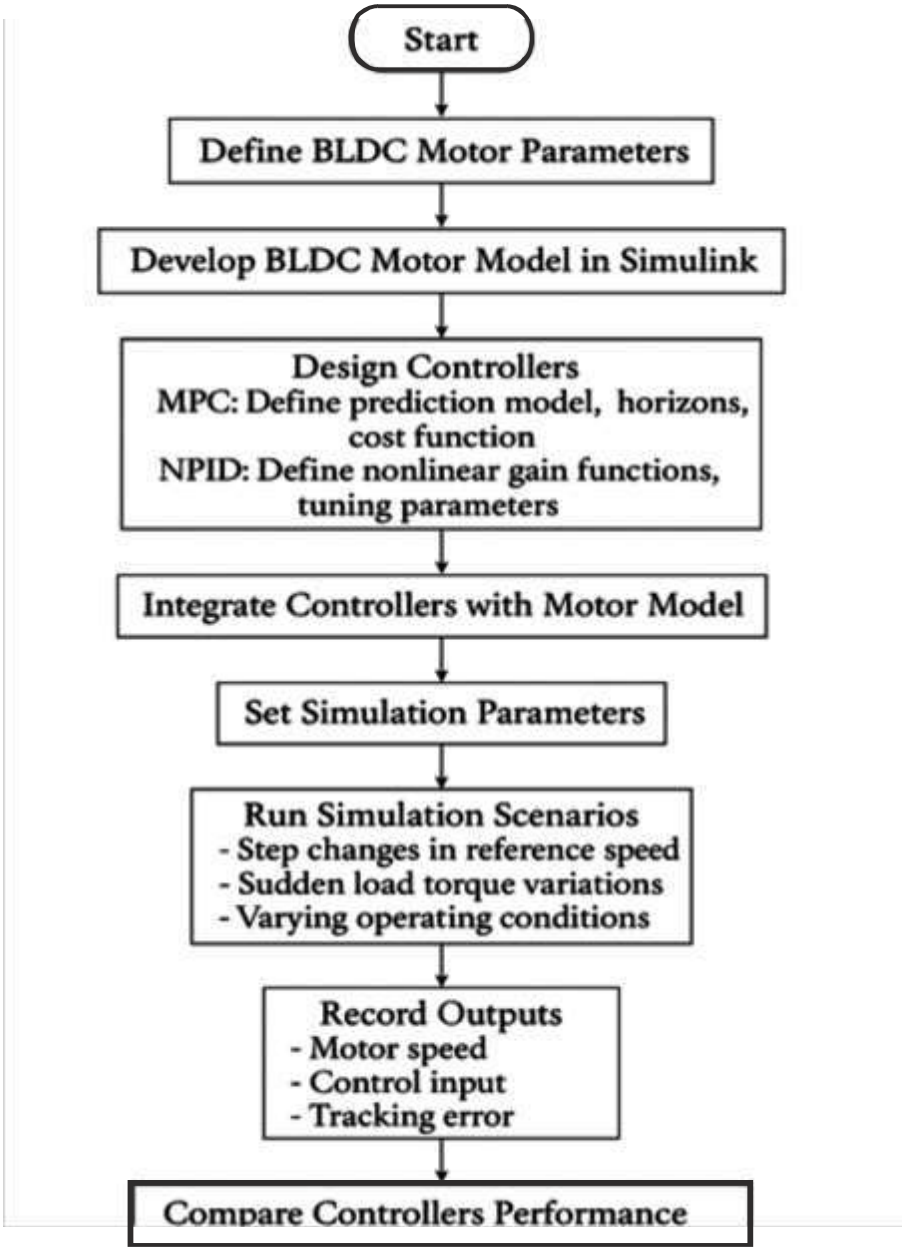

Figure 4. Simulation procedure for MPC and NPID controllers

Table 1. Simulation parameters

	Motor parameters	Values
1	Armature resistance R_a	1.0 Ω
2	Armature inductance L_a	0.046H
3	Torque constant k_t	14.48Nm/A
4	Viscous friction f	0.08Nms/rad
5	Back EMF k_b	0.55Vs/rad
6	Moment of inertia J	0.093J(kg/m^2)

However, the transfer function which was shown in equation (13) was simplified using the simulation parameters shown in Table 1. is now given as [11].

$$\frac{\Theta(s)}{E_a} = \frac{14.48}{2.44\times10^{-6}s^2 + 0.0161s + 1}$$

3.0 RESULTS AND DISCUSSION

The section presents the software simulation results of BLDC motor obtained from the research carried out using matlab/Simulink.

3.1 Software Simulation Results

A. Unit step response test

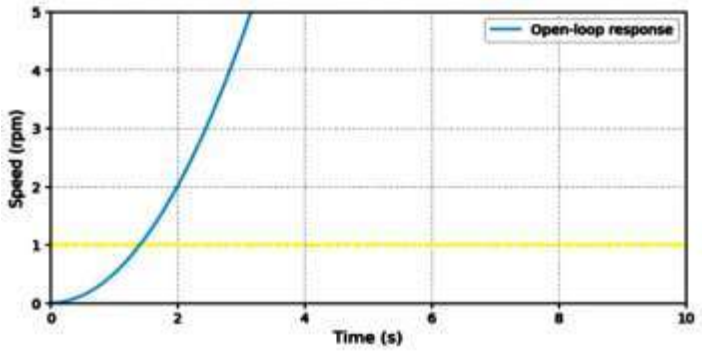

Figure 5. open loop response with step

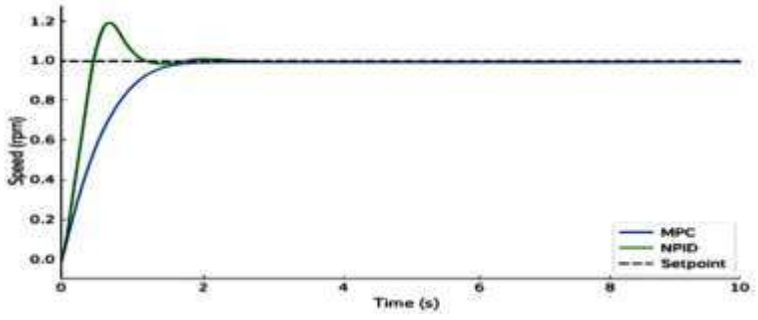

Figure 6. Performance of step response with NPID and MPC

The output waveform shown in Figure 5. highlights the performance of unit step response with NPID and MPC. The NPID controller demonstrates a faster rise time of 0.78sec but with a slight overshoot of 2.0% due to oscillation as observed in the waveform. While the MPC controller demonstrates a shorter settling time of 0.9800 and with minimal overshoot of 0.0616%. The results indicate systems requiring a precise control, sharp response, and

speed deviation reduction would consider the two controllers compared to classical controllers such as PID [3]. Step response values were given in table 2.

Table 2. Step Response

Controller	Step Response		
	Rise Time(s)	Settling Time(s)	Overshoot (%)
NPID	0.7893	1.0198	2.0930
MPC	0.8000	0.9800	0.0616
PID	0.2930	7.8600	35.232

B. Sine-waveform tracking test

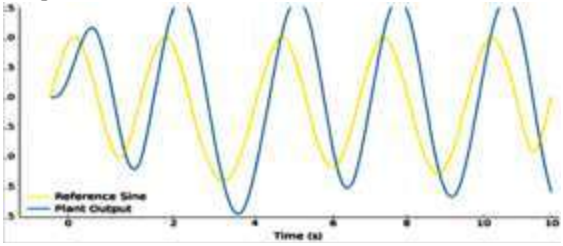

Figure 7. Open Loop Response

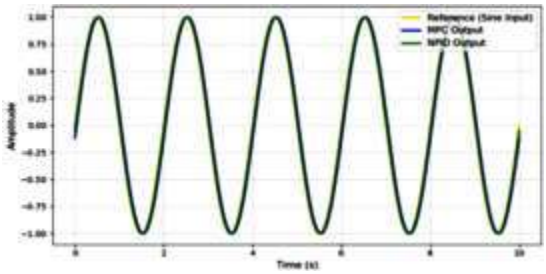

Figure 8. Closed Loop Response (MPC vs NPID)

This is a sine wave signal tracking test, whereby the set-point changes in sinusoidal form (from 0 to +1 to -1) as shown in Figure 7. The NPID controller demonstrate a good tracking accuracy with approximately 0% steady-state error. While the MPC controller shows a slightly phase mismatch with about 1.2% steady state error. However, the superior tracking accuracy of the NPID subjected to low current, mechanical torque stability, constant disturbance rejection.

C. Square waveform tracking test

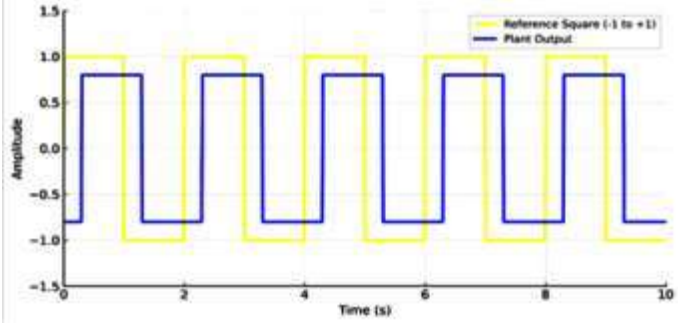

Figure 9. open loop response

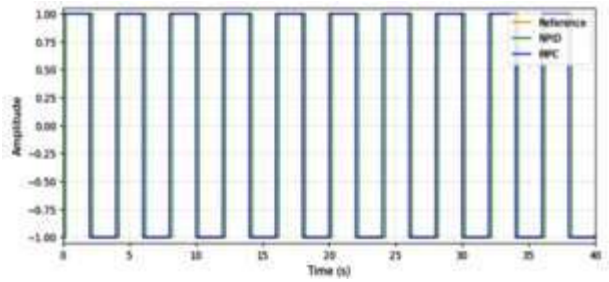

Figure 10. closed loop response (MPC vs NPID)

This is a square wave signal tracking test, whereby the set-point changes from **+**1 to -1 as shown in Figure 9**.** The NPID controller demonstrate a good tracking accuracy with minimal lag in term of shape and phase of the waveform (reference) which clearly shows the controller will be good for on/off system**.** While the MPC controller highlights a slightly poor tracking of the reference signal likewise phase/shape lagging compared to NPID**.** This signifies that both controllers can handle well an on/off systems (switch) properly compared to [15] [16]**.**

D. Ramp waveform tracking test

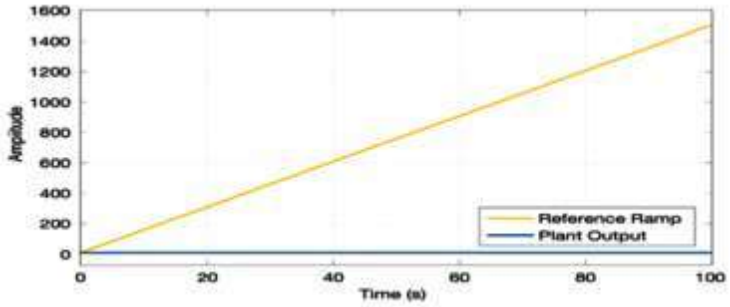

Figure 11. Open Loop Response

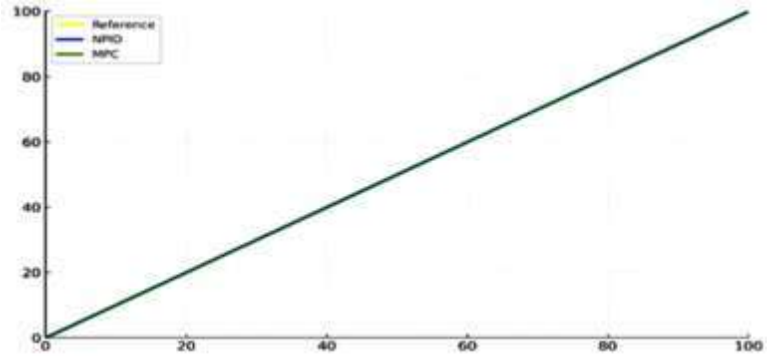

Figure 12. closed loop response (MPC vs NPID)

In the Ramp closed loop tracking test, the NPID controller demonstrate a perfect reference tracking ability with zero steady-state error as shown in Figure 11**.** while, the MPC comes with a slight error which approximately equal to 0.2%**.** However, both the two controllers demonstrate a good tracking test but the NPID is slightly ahead of MPC in-term of tracking performance and will fit the requirement of system (BLDC) especially during temperature rise, motor speed increase compared to [16]**.**

4. CONCLUSION

The paper presented a performance comparison of model predictive control (MPC) and Nonlinear PID (NPID) for BLDC motor speed control. The simulation results obtained indicate that the NPID possess a faster response with approximate value of 0.78sec, while MPC minimizes overshoot with a value of 0.0616% which offered smooth transient response. Furthermore, others test input signal were also applied to test the tracking ability of the two controllers whereby the NPID slightly outperformed the MPC when tracking the sine-waveform, square waveform and the ramp signal. This finding demonstrates the effectiveness of the advanced control techniques in handling the BLDC motor nonlinearities and parameter uncertainties.

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